PATENT

**IN THE U.S. PATENT AND TRADEMARK OFFICE**

In re application of: Yumi SAITO et al.
Conf.:
Appl. No.:
Group:
Filed: February 10, 2004
Examiner:
Title: EVALUATION WIRING PATTERN AND EVALUATION METHOD FOR EVALUATING RELIABILITY OF SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE HAVING THE SAME PATTER

**PRELIMINARY AMENDMENT**

Assistant Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

February 10, 2004

Sir:

The following preliminary amendments and remarks are respectfully submitted in connection with the above-identified application.

**Amendments to the Specification** begin on page 2 of this paper.

**Remarks** begin on page 3 of this paper.

An **Appendix** is attached following the signature page of this paper.